

**IN THE ABSTRACT**

Please replace the present abstract with the following:

**ABSTRACT OF THE DISCLOSURE**

~~An improved d~~Digital-data receiver synchronization apparatus and method is provided wherein ~~memory devices in the receiver such as phase-lock loops are provided~~ with composite phase-frequency detectors, mutually cross-connected comparison feedback means, or both to provide robust reception of digital data signals. ~~The apparatus and method are preferably utilized with synchronous architecture wherein a~~ A single master clock is can be used to provide frequency signals to the memory devices, and also can be used with asynchronous architecture. Advantages can include ~~The apparatus and method provide~~ fast lock-up time in moderately to severely noisy conditions, greater tolerance to noise and jitter when locked, and have improved tolerance to clock asymmetries.